

AOTF470

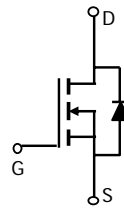
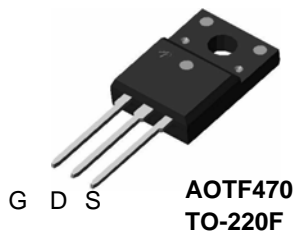
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AOTF470 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.
 -RoHs Compliant

Features

V_{DS} (V) = 75V
 I_D = 50 A (V_{GS} = 10V)
 $R_{DS(ON)} < 11.5m\Omega$ (V_{GS} = 10V)



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOTF470	Units
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	36	A
Avalanche Current ^C	I_{AR}	200	A
Repetitive avalanche energy $L=0.3mH$ ^C	E_{AR}	45	A
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	AOTF470	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	60	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	2.8	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	75			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 25\text{V}$			1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2	2.7	4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	200			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=30\text{A}$ $T_J=125^\circ\text{C}$		9.8 16.0	11.5 19.0	$\text{m}\Omega$
g_{FS}	Transconductance	$V_{DS}=5\text{V}$, $I_D=50\text{A}$		90		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=30\text{V}$, $f=1\text{MHz}$		4700	5640	pF
C_{oss}	Output Capacitance			400		pF
C_{rss}	Reverse Transfer Capacitance			180		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		3	4.5	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $I_D=30\text{A}$		114	140	nC
Q_{gs}	Gate Source Charge			33		nC
Q_{gd}	Gate Drain Charge			18		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $R_L=1\Omega$, $R_{GEN}=3\Omega$		21		ns
t_r	Turn-On Rise Time			39		ns
$t_{D(off)}$	Turn-Off Delay Time			70		ns
t_f	Turn-Off Fall Time			24		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=30\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		53	70	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=30\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		143		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A=25^\circ\text{C}$.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\ \mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

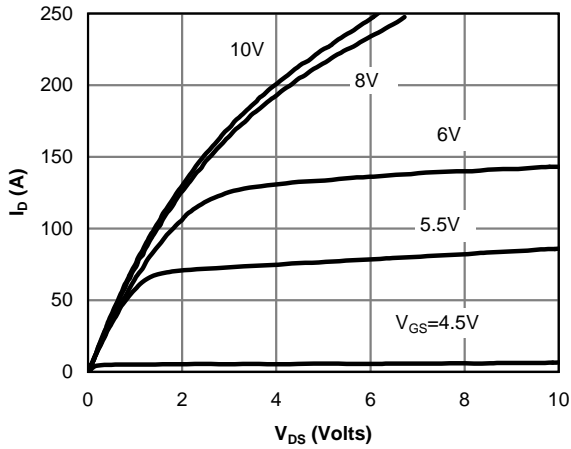


Figure 1: On-Region Characteristics

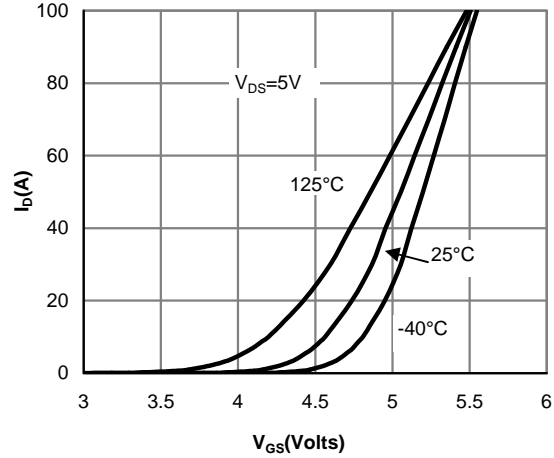


Figure 2: Transfer Characteristics

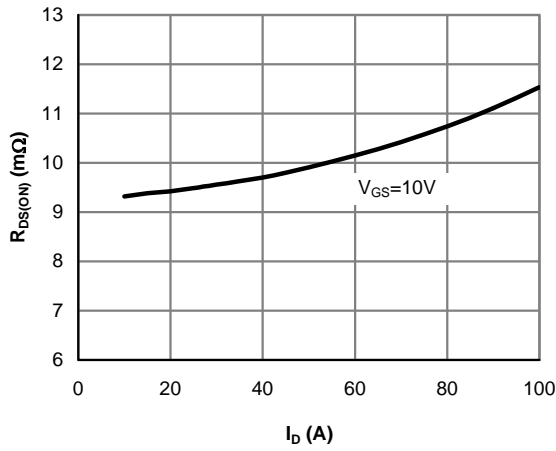


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

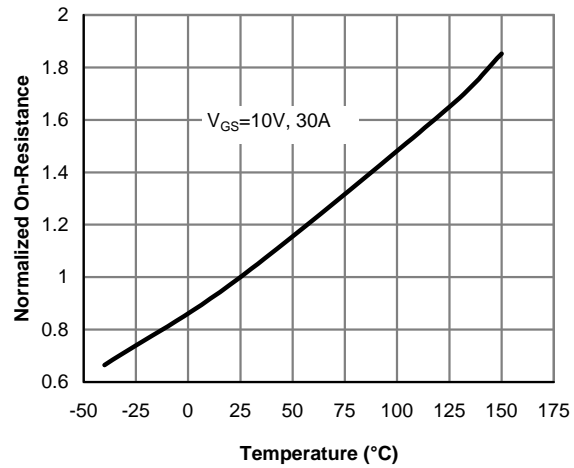


Figure 4: On-Resistance vs. Junction Temperature

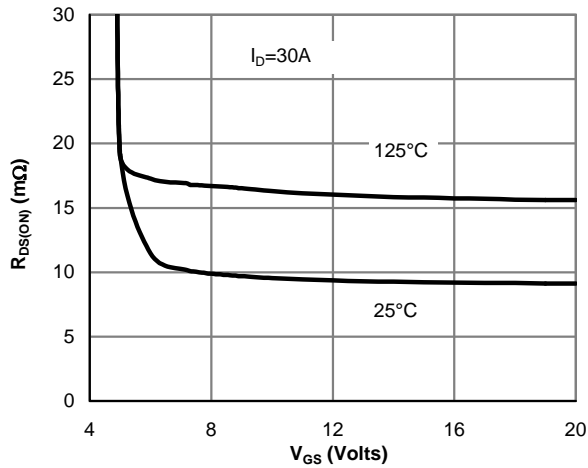


Figure 5: On-Resistance vs. Gate-Source Voltage

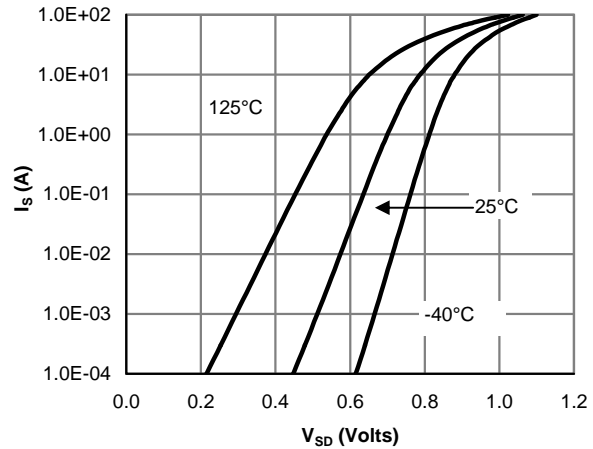


Figure 6: Body-Diode Characteristics

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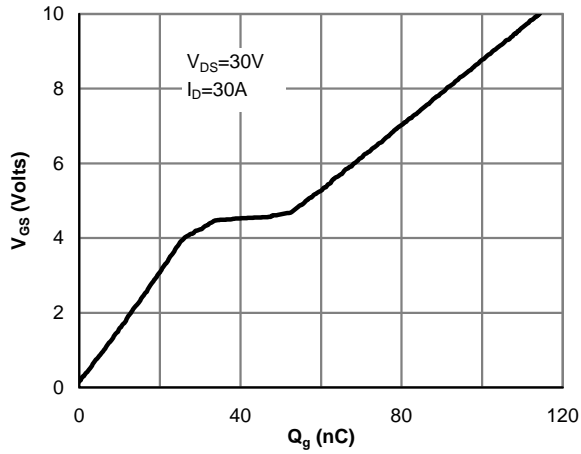


Figure 7: Gate-Charge Characteristics

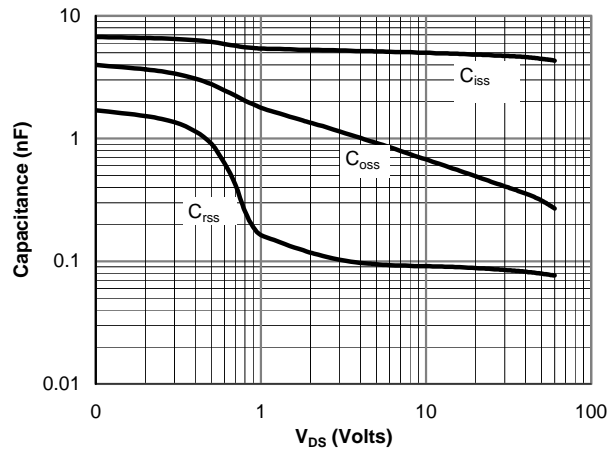


Figure 8: Capacitance Characteristics

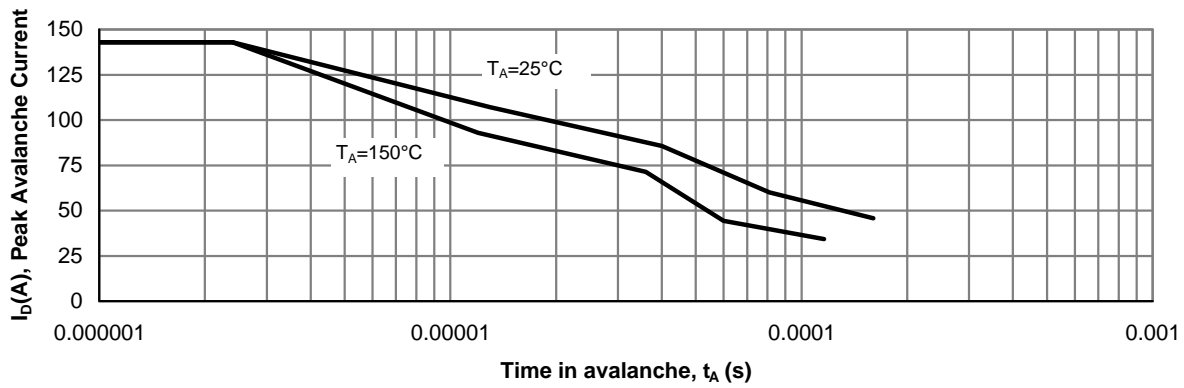


Figure 9: Single Pulse Avalanche capability

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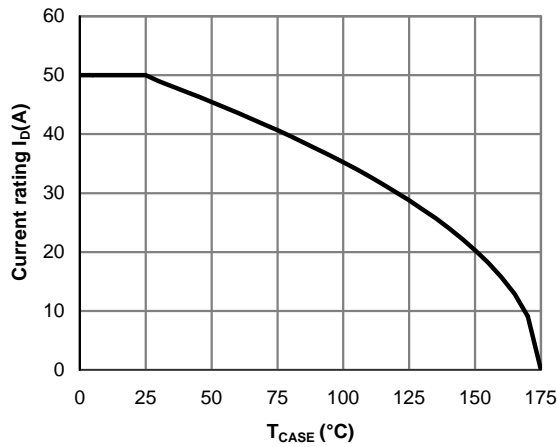


Figure 10: Current De-rating (Note B)

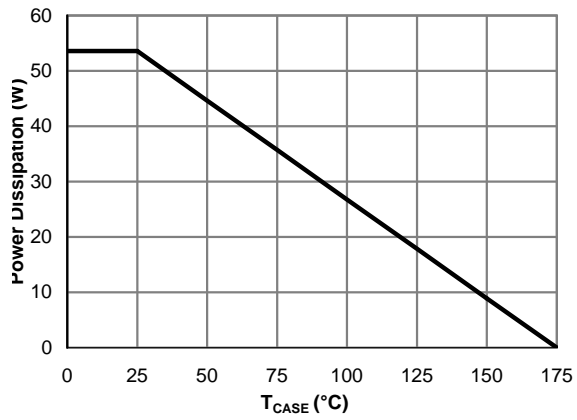


Figure 11: Power De-rating (Note B)

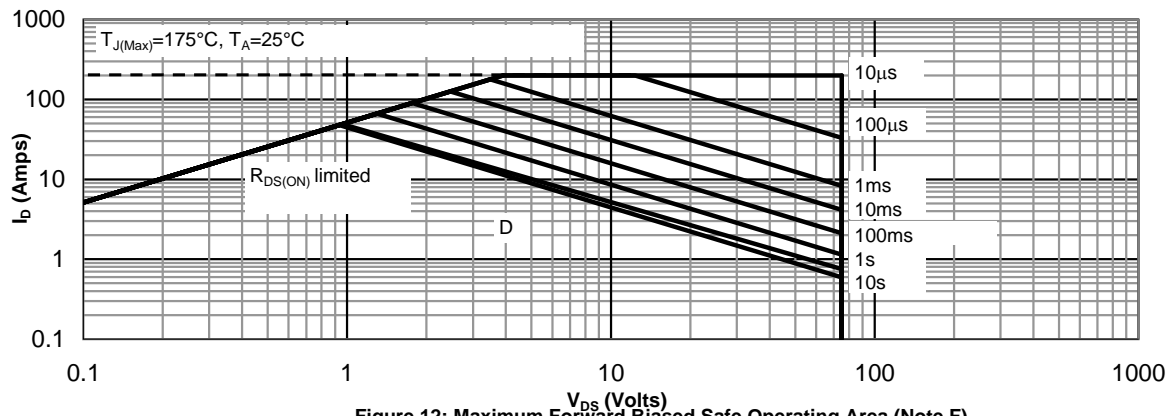


Figure 12: Maximum Forward Biased Safe Operating Area (Note F)

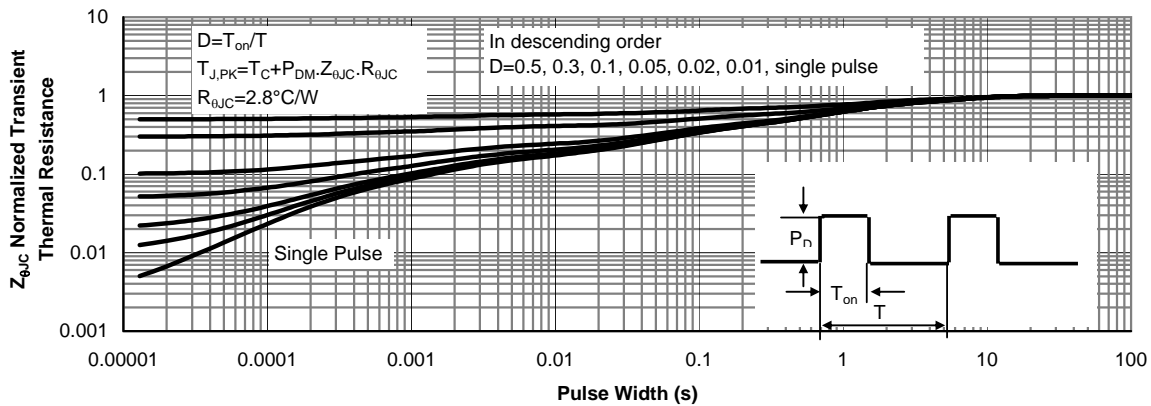


Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)